IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/652,550
Filing Date ..... August 31, 2000
Inventor ..... Keiji Jono et al.
Assignee ..... KMT Semiconductor, LTD
Group Art Unit 2811
Examiner ..... Quang D. Vu
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References –See Attached Form PTO-1449

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449, copies of which are attached. No admission is made regarding whether all the submitted references are prior art.

Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: 3-10-03

By: _____
D. Brent Kenady
Reg. No. 40,045

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. KM1-001	SERIAL NO. 09/652,550
	LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)	APPLICANT: Keiji Jono et al.	
		FILING DATE August 31, 2000	GROUP 2811

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,034,409	03/07/2000	Sakai et al.			
	AB	6,171,924 B1	01/09/2001	Wang et al.			
	AC	6,154,417	11/28/2000	Kim			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		
	AS		
	AT		

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/652,550
Filing Date ..... August 31, 2000
Inventor ..... Keiji Jono et al.
Assignee ..... KMT Semiconductor, LTD and Micron Technology, Inc.
Group Art Unit 2811
Examiner ..... Quang D. Vu
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

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Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: 2-2-04 By: _____
D. Brent Kenady
Reg. No. 40,045

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		FILING DATE August 31, 2000	GROUP 2811

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,081,662	06/27/00	Murakami et al.			
	AB	5,994,198	11/30/99	Hsu et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

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